

ABSTRACT OF THE DISCLOSURE

It is an object of the present invention to provide a structure capable of determining a failed part of a semiconductor device in sufficient detail. An n⁺ impurity region (3) and a p⁺ impurity region (4) are connected with each other and further connected with a peripheral circuit (50). A gate electrode (1) and a gate electrode (10) are connected with each other and further connected with the peripheral circuit (50). A ground potential (8) is applied to an n⁺ impurity region (2) and a p⁻ well region (6). A power source potential (9) is applied to a p⁺ impurity region (5) and an n⁻ well region (7).

5 An n⁺ impurity region (23) and a p⁺ impurity region (24) are connected with each other and further connected with the gate electrode (10) through a metal wire (31). The ground potential (8) is applied to a p⁻ well region (26) and the power source potential (9) is applied to an n⁻ well region (27).

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